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FAULT TOLERANT CMOS REALIZATION OF A MINORITY FUNCTION FOR AEROSPACE COMPUTER COMPLEXES

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In recent years, increased attention is paid to the reliability of the critical applications of digital equipment. Reliability means radiation resistance of digital equipment. For aerospace computer systems it is extremely urgent to develop radiation-resistant components. It is one way to ensure that the radiation resistance is the creation of a special architecture – RHBD (Radiation Hardened by Design). This approach includes triple redundancy (Triple Modular Redundancy, TMR). In implementing the triple redundancy to increase radiation resistance in the Xilinx FPGA Virtex used majoritarian elements based on a tristate buffer. One of the issuance of majority vote circuit for the loading sign to the pins of the FPGA is using a minority voting function. This feature ensures channel disconnection different from the other two. Only in this case, there is no conflict of signals at the outputs of buffers. Then it was realized majority function (voting by a majority). The FPGA logic elements LUT (Look Up Table) werer used for it. However, in this case FPGA logic resources were spent. CMOS implementation element vote on the minority was described. The paper proposes a fault tolerant CMOS implementation of minority voting function as separate elements in order to improve the performance of redundant circuits and do not use FPGA logic resources. Simulation of CMOS voting member in the minority is made in the circuit simulation of National Instruments Electronics Workbench Group system. Simulation confirms efficiency of the proposed element, and evaluation of the probability of failure-free operation shows its high efficiency. Winning there is a considerable range of probabilities as opposed to triple scheme that gets worse unreserved already at the probability of the order of 0.88.

Keywords: Triple Module Redundancy, Majority Vote Circuit, 3-State Buffer, Minority Function, Fault Tolerance.

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ОТКАЗОУСТОЙЧИВЫЙ ЭЛЕМЕНТ ГОЛОСОВАНИЯ ПО МЕНЬШИНСТВУ ДЛЯ АЭРОКОСМИЧЕСКИХ ВЫЧИСЛИТЕЛЬНЫХ КОМПЛЕКСОВ

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Для аэрокосмических вычислительных комплексов необходима надёжная, радиационно стойкая элементная база, в том числе программируемые логические интегральные схемы (ПЛИС – FPGA). При реализации тройного резервирования (Triple Module Redundancy – TMR) с целью повышения радиационной стойкости в FPGA Virtex фирмы Xilinx используются мажоритарные элементы на основе буферов с тремя состояниями с использованием функции голосования по меньшинству, реализованной на логических элементах LUT (Look Up Table). Предлагается отказоустойчивая КМОП-реализация функции голосования по меньшинству в виде отдельных элементов для того, чтобы повысить быстродействие резервированной схемы и не использовать логические ресурсы ПЛИС. Выполняется моделирование КМОП-элемента голосования по меньшинству в системе схемотехнического моделирования National Instruments Electronics Workbench Group.

Ключевые слова: *мажоритирование, мажоритар, функция голосования по меньшинству, буфер с тремя состояниями на выходе, отказоустойчивость.*

Introduction. In recent years special attention is paid not only to digital equipment of critical application reliability, including aerospace digital computer systems [1; 2], but also to radiation-resistant element basis [3]. The Atmel [4; 5] company is working hard on the creation of radiation-resistant chips. One of ways to ensure radiation resistance is creation of special architecture – RHBD (Radiation Hardened By Design). This approach includes triple redundancy (Triple Modular Redundancy, TMR) or majority function. Majority reservation is planted in the FPGA [6] (field-programmable gate array) programmable logic integrated circuits (PLIC) of the VirtexTM series of

Xilinx [7–9]. At the same time majority devices (Majority Vote Circuits) on the basis of 3-State buffers (BUFT) and vote devices on minority "Minoriti" (minority function, Minority Vote Circuits) are used. It is specified that vote devices on minority can be realized on the basis of so-called LUT (look up table) which represents ROM – multiplexers which inputs of data fix the given logic function [6]. Synthesis of the fault-tolerant device of vote on minority (Minority Vote Circuits) on CMOS transistors for the purpose of their use without involvement of the logical LUT resources and increase in probability of trouble-free (consistent) operation of triplicate digital system arouse interest.

Majority element based on 3-state buffers with minority function vote devices. In FPGA VirtexTM of Xilinx [7–9] realization of majority function on PLIC contact elements (programmable logical integrated circuit) using 3-state buffers and minority vote devices (Minority) is described (fig. 1, 2).

The table of "Minority" (Minority Voted) function validity of three channels A, B, C is suggested in fig. 3.

Thus the Minority Voted function has the following expression:

$$Z = \overline{A}BC \vee A\overline{B}\overline{C}. \quad (1)$$

That is (1) equals one in case of difference of this channel (A, B or C) from two others transfering the output of the corresponding buffer to the third state to avoid conflict between signals with two other buffers having identical outputs. Let's construct CMOS implementation diagram (1).

CMOS implementation of minority voted function. The suggested simplified diagram of CMOS Minority Voted function implementation (1) is represented in fig. 4.

Element modeling fig. 7 with three additional inverters in the system of circuitry modeling of National Instruments Electronics Workbench Group [10] confirms operability of the element in compliance with the table of validity fig. 3. Fig. 5 represents modeling of working (single) sets A, B, C.

Complexity of LUT [6] taking into account the setting in number of transistors (in connection with restrictions, stated in the Rules of topological design by Mead and Conway [11], n can't be more than 4) has the following appearance:

$$L_n = 2^n \cdot 8 + 2^{n+1} + 2n. \quad (2)$$

Even if for implementation of minority voting function LUT with $n = 3$ is used, we receive the following number of transistors:

$$L_3 = 2^3 \cdot 8 + 2^{3+1} + 2 \cdot 3 = 86. \quad (3)$$

The suggested implementation is complicated by the complexity of three inverters = 18 transistors, what is more than 4 times as less. However, in case of a minority voting element failure in one channel, the failure in the other channel will lead to a failure of all triplex system.

Fault tolerant CMOS realizations of voting minority function. To follow the Rules of topological design by Mead and Conway [11] on the number of sequentially switched on transistors (no more than 4) decomposition of the initial diagram is needed. One of the options is provided in fig. 6.

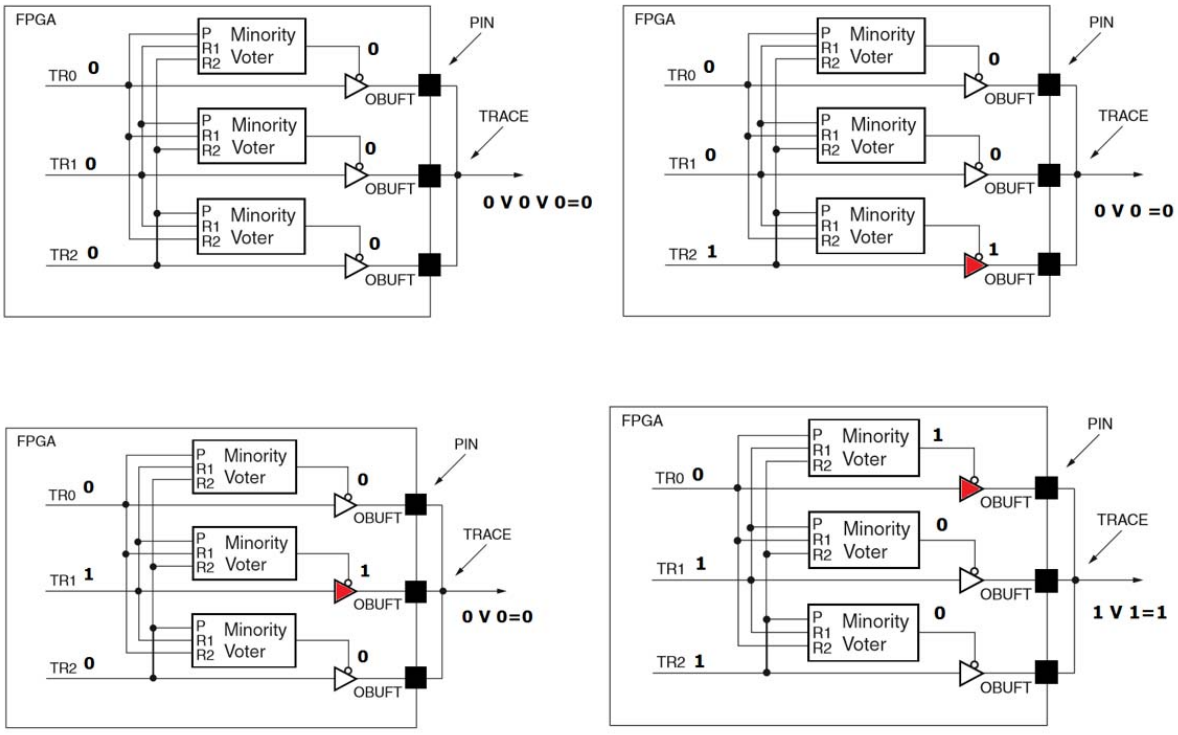


Fig. 1. Majority function implementation using "Minority" diagrams (Minority Voted) in sets 000,001, 010,011

Рис. 1. Реализация мажоритирования с использованием схем «минорити» (Minority Voted) на наборах 000,001, 010,011

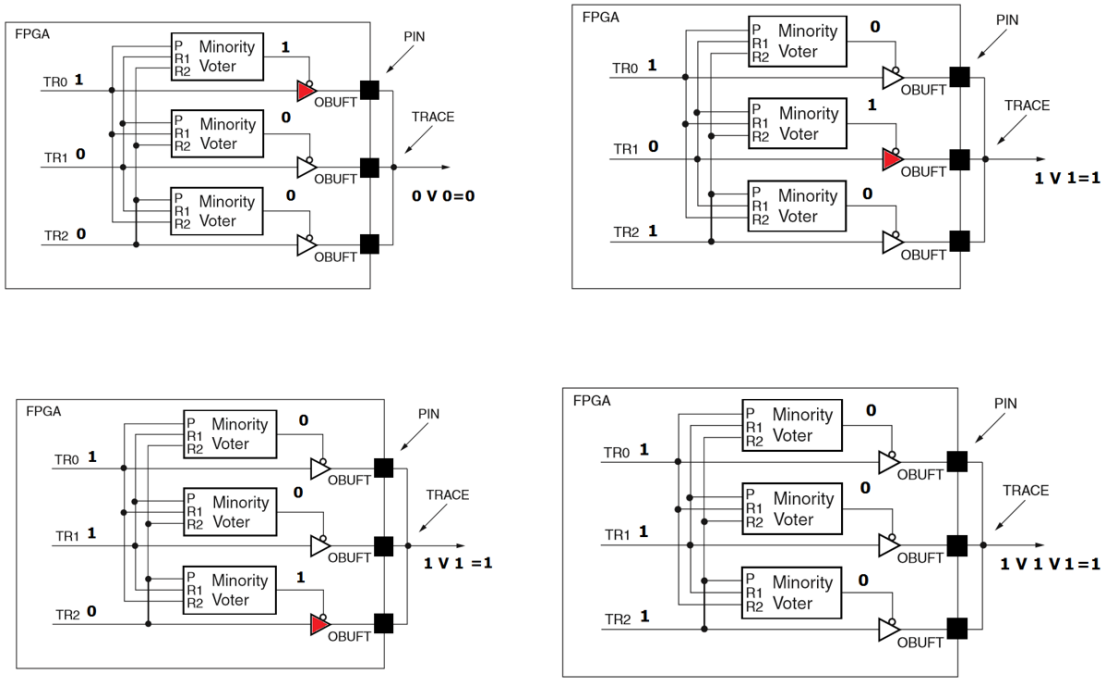


Fig. 2. Majority function implementation using “Minority” diagrams (Minority Voted) in sets 100,101, 110,111

Рис. 2. Реализация мажоритирования с использованием схем «минорити» (Minority Voted) на наборах 100,101, 110,111

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Fig. 3. The table of “Minority”
(Minority Voted) function validity

Рис. 3. Таблица истинности функции
«минорити» (Minority Voted)

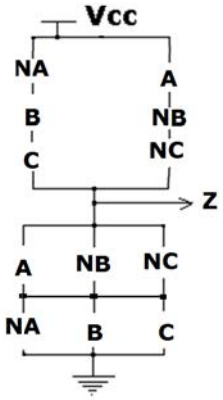
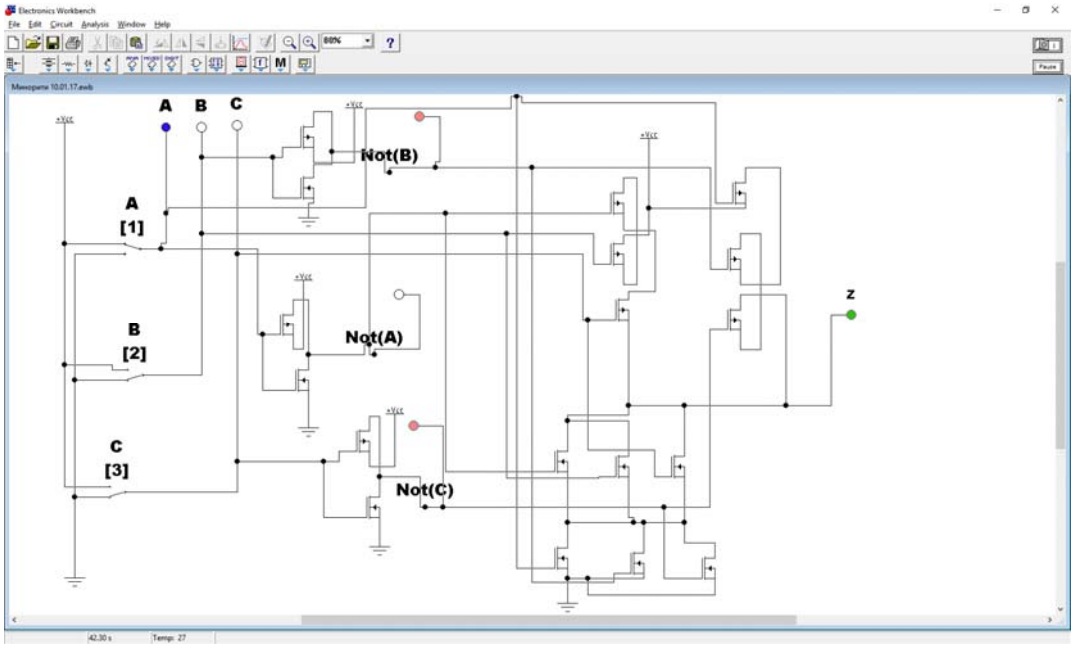
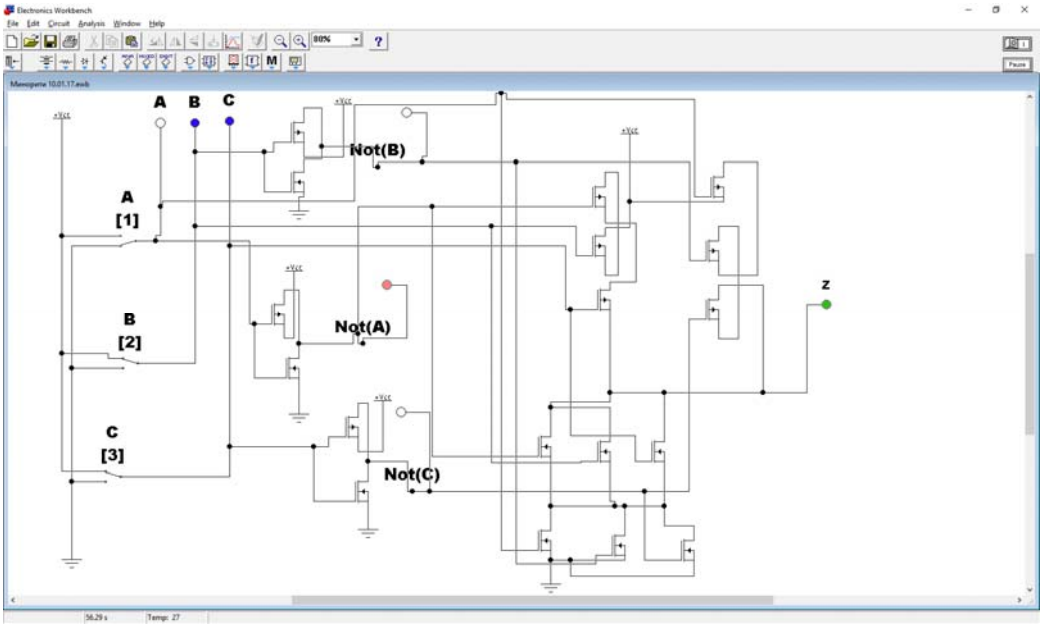


Fig. 4. Simplified diagram of CMOS
Minority Voted function implementation

Рис. 4. Упрощённая КМОП схема реализации
функции «минорити» (Minority Voted)



a



b

Fig. 5. Modeling of CMOS implementation of the minority voted element: *a* – set 100; *b* – set 011

Рис. 5. Моделирование КМОП реализации элемента голосования по меньшинству: *а* – на наборе 100; *б* – на наборе 011

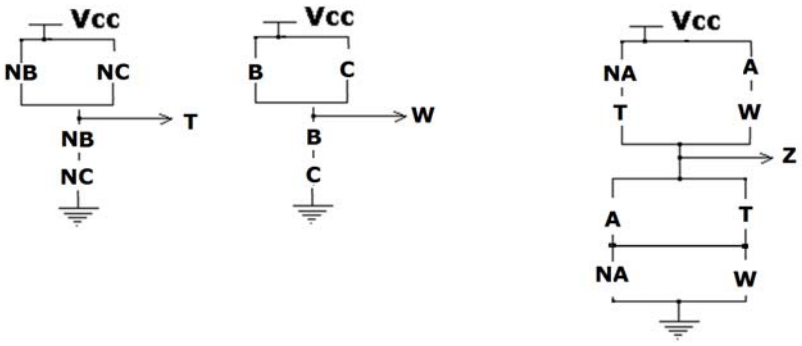


Fig. 6. Decomposition of the simplified CMOS diagram of the “Minority” function realization (Minority Voted)

Рис. 6. Декомпозиция упрощённой КМОП схемы реализации функции «минорити» (Minority Voted)

Further transistors of the decomposed diagram in compliance with [12; 13] are reserved. Simulation of the element of fig. 6 with transistor reservation and with three additional inverters on some input patterns in the system of circuitry simulation of National Instruments Electronics Workbench Group is shown in fig. 7.

Assessment of probability of failure-free operation CMOS voting on minority function realization. For the Veybull model of refusals [14] applied for the purpose of in time radiation resistance assessment of the buffer without reservation we have probability of failure-free operation:

$$e^{-(18)\lambda\cdot t^{\alpha}}, \qquad (4)$$

where failure density of one transistor, α-coefficient, $1 \le \alpha \le 2$; t – an operating time in case of radiation.

For the offered redundant scheme of the voting minority element the probability of failure-free operation will be presented by expression

$$P(t)_{\text{ftm}} = [e^{-4\cdot\lambda\cdot t^{\alpha}} + 4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{22}. \qquad (5)$$

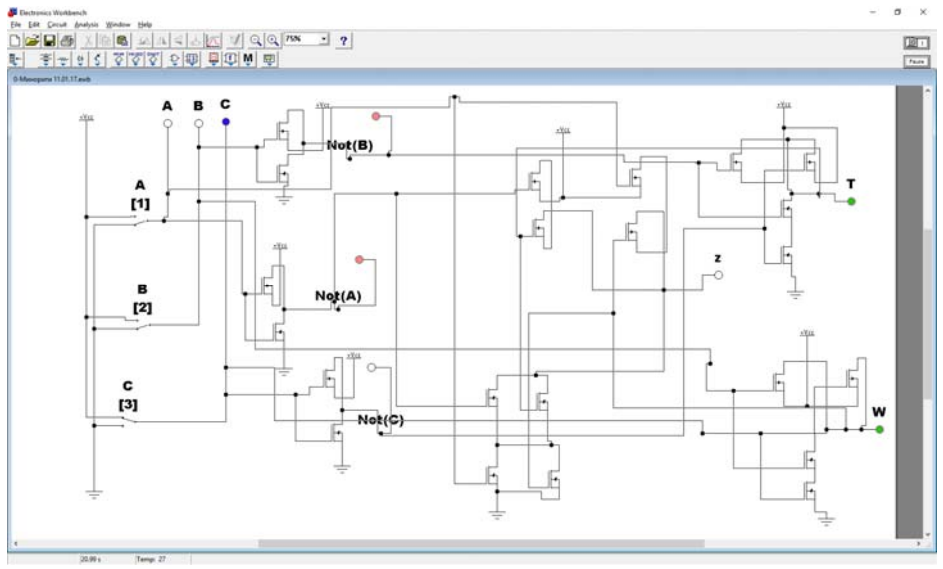
Let's estimate the tripling of the offered element. Under voting elements tripling taking into account one additional majority function:

$$P_3 = (3\cdot e^{-2\cdot(18)\cdot\lambda\cdot t^{\alpha}} - 2\cdot e^{-3\cdot(18)\cdot\lambda\cdot t^{\alpha}})e^{-(12)\cdot\lambda\cdot t^{\alpha}}. \qquad (6)$$

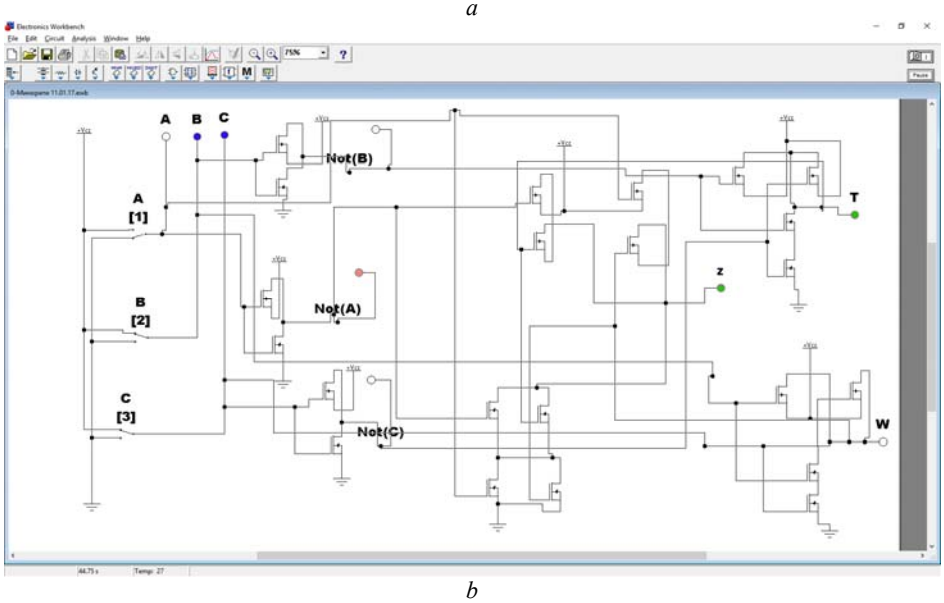
Under voting elements tripling taking into account three additional majority functions:

$$P_{33} = (3\cdot e^{-2\cdot(18)\cdot\lambda\cdot t^{\alpha}} - 2\cdot e^{-3\cdot(18)\cdot\lambda\cdot t^{\alpha}})\times \times(3\cdot e^{-2\cdot(12)\cdot\lambda\cdot t^{\alpha}} - 2\cdot e^{-3\cdot(12)\cdot\lambda\cdot t^{\alpha}}). \qquad (7)$$

Diagrams of failure free operation of minority voting element probability change without reservation, $e^{-(18)\lambda\cdot t^{\alpha}}$, of probability of failure-free operation of the offered redundant diagram, of the tripled with one majority function $P(t)_{\text{ftm}}$, of the tripled diagram P_3 with three majority functions, P_{33}, under failure rate $\lambda = 10^{-5}$ of 1/hour are represented in fig. 8.



a



b

Fig. 7. Modeling of a failure-free element of vote on minority: *a* – in set 100; *b* – in set 011

Рис. 7. Моделирование отказоустойчивого элемента голосования по меньшинству: *а* – на наборе 100; *б* – на наборе 011

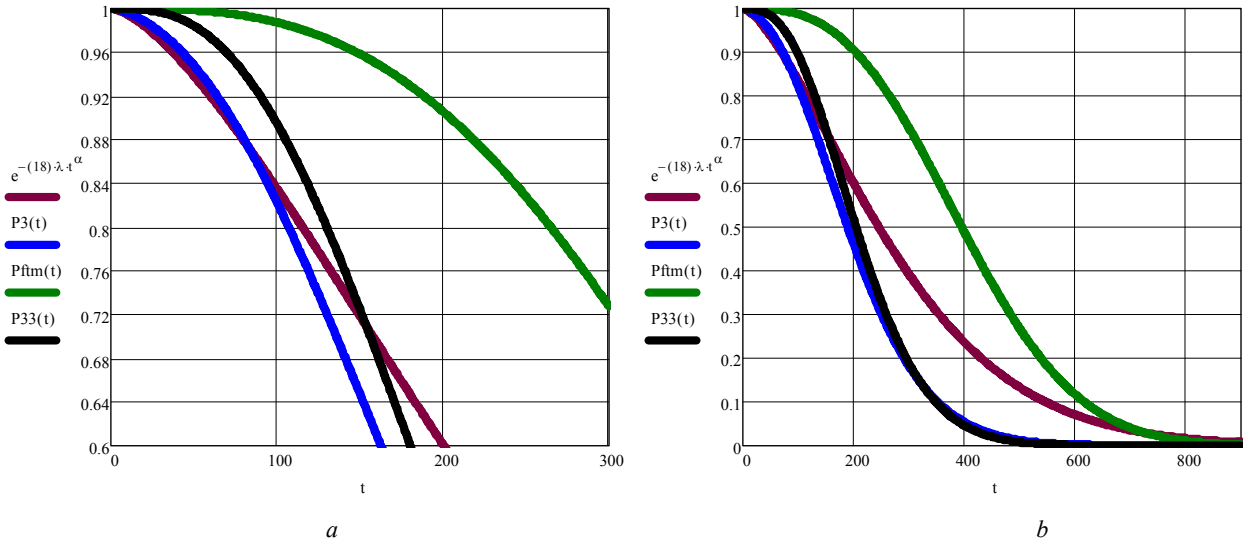


Fig. 8. Diagrams of failure-free operation of the buffer without reservation probability change $e^{-(6)\lambda \cdot t^{\alpha}}$, failure-free operation of the redundant diagram – with transistors titration $P(t)_{\text{ftm}}$, of the triple diagram with one majority function P_3, of triple diagram with three majority functions P_{33} under failure density $\lambda = 10^{-5}$ of 1/hour: *a* – in the range from 1 to 0.6; *b* – in the range of probabilities from 1 to 0

Рис. 8. Графики изменения вероятности безотказной (бессбойной) работы буфера без резервирования $e^{-(6)\lambda \cdot t^{\alpha}}$, вероятности безотказной (бессбойной) работы резервированной схемы – с расчетверением транзисторов $P(t)_{\text{ftm}}$, троированной схемы P_3 с одним мажоритаром, троированной схемы с тремя мажоритарами P_{33} при интенсивности отказов (сбоев) $\lambda = 10^{-5}$ 1/час; *а* – в диапазоне от 1до 0,6; *б* – в диапазоне вероятностей от1 до 0

Conclusion. In FPGA Virtex of Xilinx for the purpose of radiation resistance improvement tripling is used (Triple Module Redundancy – TMR). For the delivery of majority signal on FPMT connections "Minority" functions realized in three LUT are used, where the single signal is formed only in case of difference of this input from two others, providing at the buffers output which aren't in the third state, always 0 or 1 without "mixing". In the article failure-free CMOS realization of the voting minority element, allowing not to use FPMT logical resources and essentially simplify realization of a majority function on the basis of buffers, are described.

The executed modeling in the system of circuitry modeling of National Instruments Electronics Workbench Group has confirmed operability of the scheme offered.

The assessment failure-free operation probability confirms a considerable advantage over the triple diagram. This advantage is observed on the wide range of probability unlike that of the triple diagram which becomes worse than not redundant already at probability of about 0.88.

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