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DEVELOPMENT OF INTERFACE MODULE EMULATOR ARCHITECTURE FOR SPACECRAFT LIFE SUPPORT SYSTEMS

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The article gives an analysis of special characteristics of ground-based experimental evaluation of on-board radio-electronic equipment, taking the control unit of up-to date spacecraft on-board control complex as the test objective. The focus is the problem of providing testing procedures of the specific software employed in design and manufacture process. A solution of the problem is worked out on the basis of performance of a hardware-software complex which emulates interface modules for the computing module of control unit. According to the general operation algorithm of the control unit, the developed complex is regarded as a multi-user system. The main functional requirements for hardware-software emulator, regarded as the corresponding queuing system, are also defined. The results of the experiments with the computer module operation prompted the requirements for the emulator response time from the point of view of its operation stability in real strict-time mode. In order to ensure the required efficiency of operation, the emulated functions of the interface modules are classified according to the severity level of their execution determinacy. The results of experimental evaluation of the service channel hardware design variants when applying multi-functional reconfigurable input-output digital devices allowed to develop a hardware-software emulator structural circuit based on operation parallelism of programmable integrated logic circuits and flexibility of software reconfiguration. The realization of emulated functions of selected classes within the available architecture was carried out using the corresponding hardware blocks and software module. The presented analysis of the emulator response limits was performed with the application of National Instruments technologies. The results of the developed hardware-software emulator evaluation and practical application, as well as other possible ways of applying the proposed approach for tests of spacecraft on-board radio-electronic equipment and space system components were also analyzed.

Keywords: practical evaluation, spacecraft electronic equipment, multi-user system, software- hardware modeling.

РАЗРАБОТКА АРХИТЕКТУРЫ ЭМУЛЯТОРА ИНТЕРФЕЙСНЫХ МОДУЛЕЙ СОПРЯЖЕНИЯ СИСТЕМ ЖИЗНЕОБЕСПЕЧЕНИЯ КОСМИЧЕСКИХ АППАРАТОВ

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Рассмотрена специфика наземной экспериментальной отработки бортовой радиоэлектронной аппаратуры на примере блока управления бортового комплекса управления современных космических аппаратов. Сформулирована проблема обеспечения процесса тестирования его программного обеспечения в процессе проектирования и изготовления. Предложено решение обозначенной проблемы на основе аппаратно-программного комплекса, эмулирующего работу интерфейсных модулей сопряжения для вычислительного модуля блока управления. В соответствии с обобщенным алгоритмом функционирования блока управления разрабатываемый комплекс рассмотрен в виде многопользовательской системы. Определены основные функциональные требования к аппаратно-программному эмулятору как к соответствующей системе массового обслуживания. На основе проведенных экспериментальных исследований процесса функционирования вычислительного модуля

сформулированы требования к времени реакции эмулятора с точки зрения обеспечения его работы в режиме жесткого реального времени. В целях обеспечения требуемой оперативности функционирования проведена классификация эмулируемых функций интерфейсных модулей сопряжения в соответствии со степенью критичности детерминированности их выполнения. По результатам экспериментальной апробации вариантов технической реализации канала обслуживания на основе многофункциональных устройств реконфигурируемого цифрового ввода/вывода разработана структурная схема аппаратно-программного эмулятора, основанная на возможностях параллелизма выполнения операций в программируемых логических интегральных схемах и гибкости программного реконфигурирования. Реализация имитируемых функций выделенных классов в рамках предложенной архитектуры выполнена на основе соответствующих аппаратных блоков и программного модуля. Проведен анализ предельных значений времени реакции эмулятора на примере его реализации с использованием технологий National Instruments. Рассмотрены результаты апробации и внедрения разработанного аппаратно-программного эмулятора, а также дальнейшие направления прикладного применения предложенного подхода в процессе испытаний бортовой радиоэлектронной аппаратуры космических аппаратов и компонентов космических систем.

Ключевые слова: испытания, бортовая радиоэлектронная аппаратура, многопользовательская система, программно-аппаратное моделирование.

Introduction. Hardware-software complex for life support systems control of up-to date long-life spacecraft (SC) are subject to strict requirements concerning their trouble-free operation under destabilizing effects of the open space. One of the units of spacecraft (SC) on-board control complex designed at JSC "Academician M. F. Reshetnev "Information Satellite Systems" features a control unit (CU) comprising a processor module (PM) with a set of interface modules (IM) controlling the corresponding SC systems, components and/or assemblies (reaction-control system, thermal control system, electrical power system, pyro control units, actuators, etc.).

Problem description. Complexity of the PM software operation algorithm and several operating mode options (regular mode, on-board attitude control, etc.) required development of a specialized test complex applicable for ground testing and evaluation [1]. As a rule, the CU PM is a unified module, and the interface modules are made with regard for specific configuration of the corresponding SC service systems; that accounts for significant divergence of the software versions. Data exchange of the SC onboard central computer complex and CU PM is possible, for example, via a multiplex exchange channel, and the exchange of PM and IM is supported by a special internal data exchange interface (IDEI) [1; 2]. This exchange attachment operates special microcircuits or IP-cores, installed in field-programmable gate arrays (FPGA) of IM and performing the functions of the corresponding internal data exchange interface controllers (IDEIC). Fig. 1 presents general block diagram of the control unit.

The PM software testing procedure provides for the possibility of issuing external commands for the PM and the need to ensure two-way data communication of the PM and the corresponding IMs (fig. 1). This dictates the need for ready-made IM units connected to PM, usually featuring many hardware design and operation algorithm variants aimed for different SC. Meeting these requirements in PM software evaluation at the design stage is sometimes impossible, and cost-ineffective anyway, as it induces high expenses for supplying additional IMs [1].

Problem solving description. The problem of providing PM software advanced testing without IM can be solved by applying a special hardware-software complex emulating their performance within the CU. Here are the requirements for the emulator under development.

When the control unit installed in the spacecraft on-board control complex operates at time intervals and in sequence determined by the online leg of PM software algorithm, and by external command sources (OCCC, test instrument system, etc.), processor module of the control unit supports data exchange with corresponding interface modules through internal data exchange interface. Data exchange is performed by calling the corresponding software modules which in their turn call the IMs. Normally, calling each IM involves data recording in control registers – *control data words*, followed by reading the content of IM status register – *status data words*, displaying the issued control inputs execution and current SC systems and components status. Analysis of the state data words is followed by the execution of the corresponding leg of PM software algorithm. Let the control data words generated by the PM software be denoted by the set:

$$\boldsymbol{K}_{\mathrm{DW}} = \left\{ K_i \middle| i = 1, I \right\}, \quad (1)$$

where I – the number of IM installed in CU; K_i – control data words subset, generated by the respective software module for i IM.

IM-generated status data words are presented in the form of the set:

$$\boldsymbol{Z}_{\mathrm{DW}} = \left\{ Z_i \middle| i = 1, I \right\}, \quad (2)$$

where Z_i – status data words subset, generated by i IM.

Thus, conversion of IM control data words subset K_i into status data words subset Z_i can be generally expressed as follows:

$$Z_i = f_i\left(K_i\right), \quad (3)$$

where f_i – ratio function, generally describing the corresponding conversion ($f_i : K_i \mapsto Z_i$). The type of f_i function and the form of its presentation is determined by the functional purpose, hardware design and logic of the corresponding IM.

The collection of ratio functions f_i forms the set:

$$\boldsymbol{F}_{\mathrm{DW}} = \left\{ f_i \middle| i = 1, I \right\}, \quad (4)$$

where $\boldsymbol{F}_{\mathrm{DW}}$ – set of control data words conversions, realized by the corresponding interface modules installed in the control unit.

In accordance with the introduced designations (expressions (1)–(4)), the developed interface module emulator must ensure the realization of $\boldsymbol{F}_{\text{DW}}$ conversion functions set for control data words set $\boldsymbol{K}_{\text{DW}}$ generated by the corresponding software modules of the PM software and entering through the internal data exchange interface at random times (fig. 1). In this case, according to the PM software general logic, new control data words are not transferred to the corresponding IM until the status data words generated on the results of the execution of the previous ones are read, or their generation waiting time is not exceeded [2].

In view of the above, the developed IM hardware-software emulator can be regarded as a *multi-user system* operating in an interactive dialogue mode [3–5]. In this system:

– *user terminals (sources of requests)* are PM software modules that generate and exchange data with the corresponding interface modules;

– *requests* are control data words recorded in the corresponding registers;

– *request processing* means performing the conversion of control data words into status data words;

– *response* means status data words generated in the corresponding registers.

General block diagram of the developed interface module emulator as a corresponding closed queuing system is shown in fig. 2 [3; 4].

The main objectives of the queuing system design the article deals with (fig. 2) is the development of its structure and analysis of the main approaches to realization of a service channel aimed at ensuring the required response time $\tilde{t}_{\text{r}}$. The emulator response time $\tilde{t}_{\text{r}}$ is the sum of the in-coming control data words queuing time ($\boldsymbol{K}_{\text{DW}}$ set) – $\tilde{t}_{\text{q}}$ and the generation time of status data words ($\boldsymbol{Z}_{\text{DW}}$ set) – $\tilde{t}_{\text{s}}$ in correlation with conversion functions set $\boldsymbol{F}_{\text{DW}}$ (fig. 2).

The results of experiments with operation of the control unit processor module carried out on the basis of the ground-based debugging complex of onboard electronic equipment [1] helped to determine the following characteristic features of the queuing system shown in fig. 2:

1. The presence of several types of control data words K_i (see expression (1)), generated by the corresponding software modules, and the related time constraints imposed on the generation efficiency of the state data words Z_i.

2. Large-scale change of the time intervals between retransmitted calls to IM (for example, from 10 us to 200 ms), the probable values of which depend on: the online leg of the PM software algorithm; hardware design and current configuration of the corresponding IM; the current status of SC systems, components, assemblies; CU operation mode [1; 2].

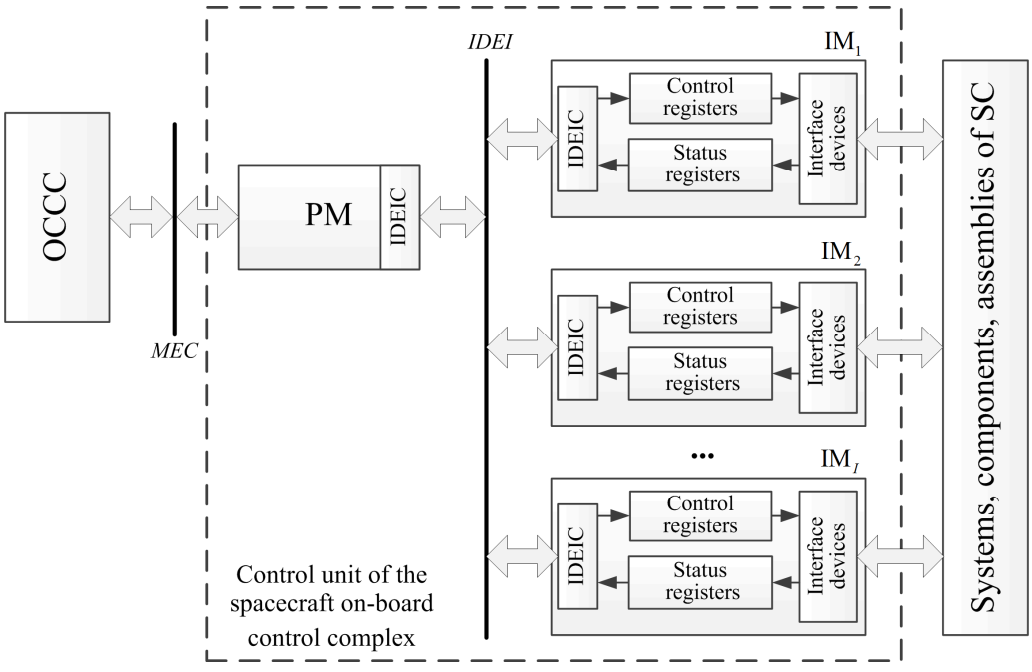

Fig. 1. General block diagram of the control unit of the on-board control complex:
PM – processor module; IDEI – internal data exchange interface; IDEIC – internal data exchange interface controller; *I* – number of control unit interface modules; OCCC – onboard central computer complex; MEC – multiplex exchange channel

Рис. 1. Обобщенная структурная схема блока управления бортового комплекса управления:
ВМ – вычислительный модуль; ВПИ – внутриприборный интерфейс обмена данными; КВПИ – контроллер внутриприборного интерфейса обмена; *I* – число интерфейсных модулей сопряжения блока управления; БЦВК – бортовой центральный вычислительный комплекс; МКО – мультиплексный канал обмена

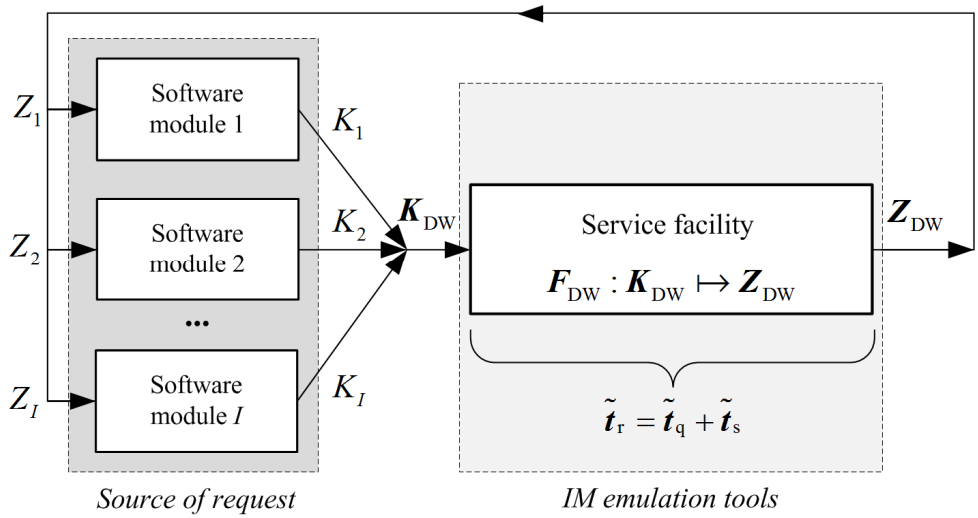

Fig. 2. General block diagram of the interface module emulator as a queuing system

Рис. 2. Обобщенная структурная схема эмулятора интерфейсных модулей сопряжения как системы массового обслуживания

The analysis of the initial data for IM design, and also for PM software design, helped to determine the following integrated classes of control data words $\boldsymbol{K}_{\text{DW}}$:

– *Class № 1*. The time required by the emulator for generating status data words in the corresponding registers is not more than 12 us ($\tilde{t}_{\text{r}}^{\text{K1}} \le 12$ us);

– *Class № 2*. The time required by the emulator for generating status data words in the corresponding registers exceeds 12 us, but is not more than 150 ms (12 us < $\tilde{t}_{\text{r}}^{\text{K2}}$ < 150 ms).

Thus, in accordance with the determined special characteristics, hardware-software emulator of interface modules as a closed queuing system must ensure the in-coming request processing determinacy specified by $\tilde{t}_{\text{r}}^{\text{K1}}$ and $\tilde{t}_{\text{r}}^{\text{K2}}$ values, i. e. realization of real strict-time mode related to PM internal processes in the situation of incomplete empirical data on the incoming traffic parameters [6].

Preliminary evaluation of the service channel based on the programmable integrated logic circuit of the reconfigurable digital input-output device in the form of functional hardware registers linked to the IP- core of the internal interface controller revealed its low processing speed of class No.1 control data words. The corresponding time the control computer requires for reading $\boldsymbol{K}_{\text{DW}}$, program conversion $\boldsymbol{F}_{\text{DW}} : \boldsymbol{K}_{\text{DW}} \mapsto \boldsymbol{Z}_{\text{DW}}$, and recording $\boldsymbol{Z}_{\text{DW}}$ values into respective FPGA registers, designed with account for breaks formed with entry of new $\boldsymbol{K}_{\text{DW}}$ values, made 10–15 ms (i. e. $\tilde{t}_{\text{s}}$ = 10–15 ms) regardless of control data words queuing time.

To ensure the required performance efficiency, a combined emulator architecture based on the features of FPGA operational parallelism and program reconfiguration flexibility was worked out [2; 7]. With the account for the revealed discontinuity of control data words generated by PM and the given classification of speed requirements for status data words generation, $\boldsymbol{K}_{\text{DW}}$ and $\boldsymbol{Z}_{\text{DW}}$ sets can be presented as follows:

$$\boldsymbol{K}_{\text{DW}} = \boldsymbol{K}_{\text{DW}}^{\text{K1}} \cup \boldsymbol{K}_{\text{DW}}^{\text{K2}}, \qquad \boldsymbol{Z}_{\text{DW}} = \boldsymbol{Z}_{\text{DW}}^{\text{K1}} \cup \boldsymbol{Z}_{\text{DW}}^{\text{K2}},$$

where $\boldsymbol{K}_{\text{DW}}^{\text{K1}}$ and $\boldsymbol{K}_{\text{DW}}^{\text{K2}}$ – IM-emulated control data words sets, belonging to the selected classes № 1 and № 2; $\boldsymbol{Z}_{\text{DW}}^{\text{K1}}$ and $\boldsymbol{Z}_{\text{DW}}^{\text{K2}}$ – IM-emulated status data words sets, belonging to the selected classes №1 and №2. Respectively:

$$\boldsymbol{K}_{\text{DW}}^{\text{K1}} = \bigcup_{i=1}^{I} K_i^{\text{K1}}, \quad \boldsymbol{Z}_{\text{DW}}^{\text{K1}} = \bigcup_{i=1}^{I} Z_i^{\text{K1}}$$

$$\boldsymbol{K}_{\text{DW}}^{\text{K2}} = \bigcup_{i=1}^{I} K_i^{\text{K2}}, \quad \boldsymbol{Z}_{\text{DW}}^{\text{K2}} = \bigcup_{i=1}^{I} Z_i^{\text{K2}}$$

where $K_i^{\text{K1}}, K_i^{\text{K2}}$ and $Z_i^{\text{K1}}, Z_i^{\text{K2}}$ – control data words subsets and generated on their basis state data words subsets, belonging to the selected classes № 1 and № 2 for each i IM. At that $K_i^{\text{K1}}, K_i^{\text{K2}} \subset K_i$; $Z_i^{\text{K1}}, Z_i^{\text{K2}} \subset Z_i$ (see expressions (1), (2)).

In a similar way, functional separation of conversion functions set $\boldsymbol{F}_{\text{DW}}$ of the selected classes of the processed control data words is performed:

$$\boldsymbol{F}_{\text{DW}} = \boldsymbol{F}_{\text{DW}}^{\text{K1}} \cup \boldsymbol{F}_{\text{DW}}^{\text{K2}},$$

$$\boldsymbol{F}_{\text{DW}}^{\text{K1}} = \bigcup_{i=1}^{I} f_i^{\text{K1}}, \; f_i^{\text{K1}} \subset f_i,$$

$$\boldsymbol{F}_{\text{DW}}^{\text{K2}} = \bigcup_{i=1}^{I} f_i^{\text{K2}}, \; f_i^{\text{K2}} \subset f_i. \qquad (5)$$

The developed block diagram of the interface modules hardware-software emulator, taking into account the experimentally revealed discontinuity of the processed control data words, is shown in fig. 3; it comprises a multifunctional unit for reconfigurable digital input-output from FPGA, controlled by the respective industrial computer [8].

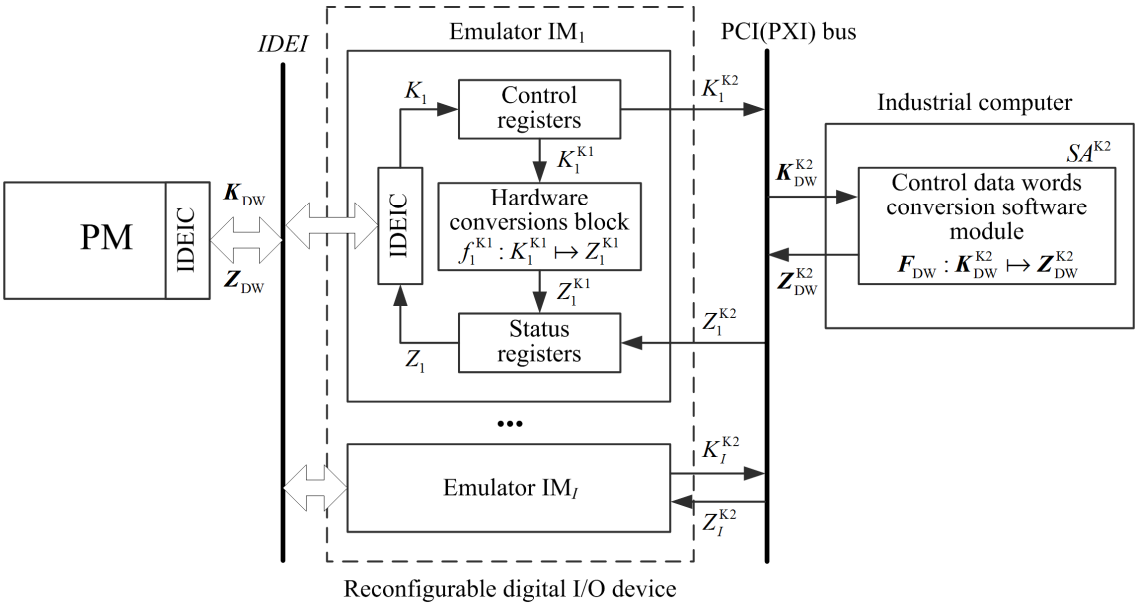

Fig. 3. General block diagram of the interface modules hardware-software emulator of SC life support system

Рис. 3. Обобщенная структурная схема аппаратно-программного эмулятора интерфейсных модулей сопряжения систем жизнеобеспечения космического аппарата

General representation of the developed hardware-software interface modules emulator as queuing systems used in processing the corresponding requests (control data words) of № 1 and 2 classes is shown in fig. 4 and 5 respectively [3; 4].

In accordance with the chosen approach, individual service channels realizing ratio functions f_i^{K1} for class No. 1 control data words (see expression (5)) come in the form of hardware conversion units making use of FPGA resources (see fig. 3). This approach ensures determinacy of Z_i^{K1} generation delays and possibility of setting up parallel individual service channels for several emulated interface modules within a single FPGA of the applied reconfigurable digital input-output device.

Ratio functions conversions specified by the $\boldsymbol{F}_{\text{DW}}^{\text{K2}}$ set (see expression (5)) are realized by the application of the top-level program module SA^{K2}, installed in an industrial computer (see fig. 3). When new K_i^{K2} values enter the control registers, a single interrupt queue is formed for all emulated IMs; in the order of their generation, interrupts are processed in the general software module SA^{K2} by way of reading K_i^{K2}, their conversion and recording Z_i^{K2} in the corresponding hardware registers of FPGA linked with SWUI IP-cores.

The analysis of the probabilistic and temporal characteristics of queuing systems presented in fig.4 and 5 can be performed on the basis of standard approaches [3–5; 9; 10]. Taking into account the necessity of ensuring the developed emulator performance in real strict-time mode ($\tilde{t}_{\text{r}}^{\text{K1}} \le 12$ us, 12 us $< \tilde{t}_{\text{r}}^{\text{K2}} < 150$ ms) we analyze the worst situation of delays in status data words $\boldsymbol{Z}_{\text{DW}}^{\text{K1}}$ and $\boldsymbol{Z}_{\text{DW}}^{\text{K2}}$ generation through the example of the developed emulator approbation in IROBO-4000 industrial computer and PCI-7813R device [2; 8].

Class № 1 requests service (performing $\boldsymbol{F}_{\text{DW}}^{\text{K1}} : \boldsymbol{K}_{\text{DW}}^{\text{K1}} \mapsto \boldsymbol{Z}_{\text{DW}}^{\text{K1}}$ conversion) is carried out by means of already developed parallel service devices, the number of which equals the IM number (see fig. 4).

Here the service device is thought of as SWUI IP - core with the corresponding hardware conversion unit making use of FPGA resources. The number of service devices for $\boldsymbol{K}_{\text{DW}}^{\text{K1}}$ equals the number of IMs in the control unit; that excepts the accumulation of entering requests in the queue; thus, the emulator response time is determined by their service time. For the queuing system presented in fig. 4, the service time of *requests* is determined only by the time of the corresponding data words generation in status registers, and for the given hardware-software emulator implementation variant based on the results of the corresponding FPGA project development the time equals 2 clock-cycles [11–13]:

$$\tilde{t}_{\text{r}}^{\text{K1}} = \tilde{t}_{\text{s}}^{\text{K1}} = 2 \cdot \frac{1}{f_{\text{cs}}} = 2 \cdot \frac{1}{40 \cdot 10^6} = 50 \cdot 10^{-9} \text{ s},$$

where f_{cs} – operational clock speed of FPGA project.

When new control data word values K_i^{K2} of No. 2 request class enter the corresponding hardware registers, a unified queue of hardware interrupts is formed for all emulated IMs. The interrupts data are processed in the SA^{K2} software module in the order of their generation (conversion $\boldsymbol{F}_{\text{DW}}^{\text{K2}} : \boldsymbol{K}_{\text{DW}}^{\text{K2}} \mapsto \boldsymbol{Z}_{\text{DW}}^{\text{K2}}$). Maximum delay of

state data words Z_i^{K2} generation when I = 8, caused by control data words K_i^{K2} accumulation due to queuing in interrupt processing (see fig. 5) may be determined on account of the above evaluation results of the service channel implementation; the resulting expression is [3–5]:

$$\max\left(\tilde{\boldsymbol{t}}_{\mathrm{r}}^{K2}\right) = \max\left(\tilde{\boldsymbol{t}}_{\mathrm{q}}^{K2}\right) + \max\left(\tilde{\boldsymbol{t}}_{\mathrm{s}}^{K2}\right) =$$

$$= (I-1)\cdot\max\left(\tilde{\boldsymbol{t}}_{\mathrm{s}}^{K2}\right) + \max\left(\tilde{\boldsymbol{t}}_{\mathrm{s}}^{K2}\right) = 8\cdot 15\cdot 10^{-3} = 120\cdot 10^{-3}\ \mathrm{s}.$$

Thus, the maximum values of response time in status data words generation for $\boldsymbol{K}_{\mathrm{DW}}^{K1}$ and $\boldsymbol{K}_{\mathrm{DW}}^{K2}$ obtained in use of the specified hardware-software IM emulator architecture meet the requirements formulated according to the experimental evaluation of PM CU performance. The suggested emulator architecture allows for modification of the implemented in SA^{K2} program module ratio sets $\boldsymbol{F}_{\mathrm{DW}}^{K2}$ avoiding the FPGA project recompilation, thus providing its flexibility and unification for further industrial application.

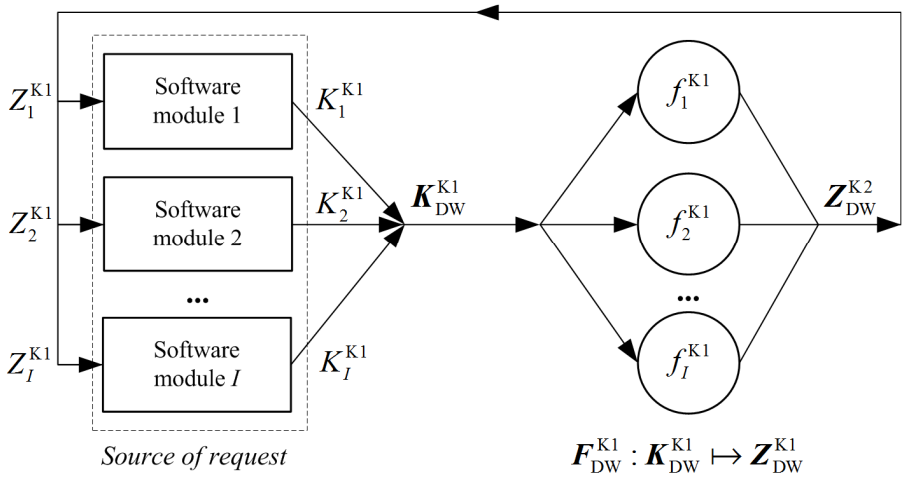

Fig. 4. Representation of the hardware-software interface modules emulator as a queuing system for processing of class No. 1 control data words

Рис. 4. Представление аппаратно-программного эмулятора интерфейсных модулей сопряжения в виде системы массового обслуживания при обработке слов данных управления класса № 1

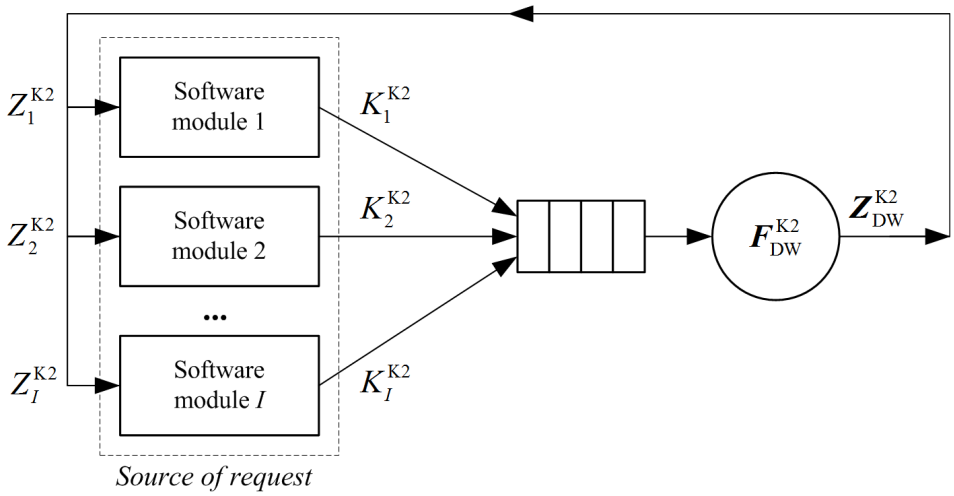

Fig. 5. Representation of the hardware-software interface modules emulator as a queuing system for processing of class No. 2 control data words

Рис. 5. Представление аппаратно-программного эмулятора интерфейсных модулей сопряжения в виде системы массового обслуживания при обработке слов данных управления класса № 2

Conclusion. The proposed know-how (fig. 3) has been evaluated and successfully put into operation at the department of astrionics design and test operations of spacecraft control systems in SC "Academician M. F. Reshetnev "Information Satellite Systems" within the ground-based debugging complex of onboard electronic equipment [1; 2; 14; 15]. The debugging complex facilities emulating control unit interface modules of the SC onboard control complex with application of the proposed approach feature a set of unified devices (hardware modules) and the corresponding "FPGA firmware" (developed IMs) that can be independently modified and then compiled in arbitrary order within the corresponding device [11–13].

Application of the PCI-7813R reconfigurable digital input-output board allowed emulation of eight interface modules of the control unit; that reduced the cost of PM software evaluation by several times and shortened its testing time. Further operation of the developed hardware-software emulator proved that the used approaches and developed techniques were correct and efficient [11–15]. The developed hardware-software emulator provides for practical evaluation of regular PM software in the environment simulating real operating conditions of SC; that was achieved by applying certain methods simulating inflight contingency situations for onboard radio-electronic equipment and spacecraft: a number of faults, such as internal interface exchange errors, one of the IMs partial malfunction or failure, SC unit/component/ assembly malfunction, etc. [14; 15].

In general, the evaluated approaches to the method of software and hardware modeling with FPGA application can also be valid for analysis of space systems operation when using special units (components) of ground-based and / or onboard electronic equipment for simulating the changing conditions of transmitting signals via communication channels that depend on the propagation medium, payload characteristics, SC path, etc. [16–18].

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